

1 WHAT IS CLAIMED IS

2

3 1. A memory structure comprising:

4 a source region of a first conductivity type;

5 a drain region of said first conductivity type;

6 a first channel region of a second conductivity type opposite  
7 said first conductivity type, located adjacent said source  
8 region;

9 a second channel region of said second conductivity type  
10 opposite said first conductivity type, located adjacent said  
11 drain region;

12 a transfer channel region of said second conductivity type,  
13 located between said first and second channel regions;

14 a first floating gate located above said first channel  
15 region;

16 a second floating gate located above said second channel  
17 region;

18 a first control gate located above said first floating gate,  
19 serving as a steering element associated with said first floating  
20 gate;

21 a second control gate located above said second floating  
22 gate, serving as a steering element associated with said second  
23 floating gate;

24 a third control gate located above said transfer channel  
25 region, serving as a control gate of an access transistor, said  
26 third control gate also overlying at least a portion of said  
27 first and second control gates;

28 a first tunneling zone formed between said first floating  
29 gate and said third control gate, and including one or more of  
30 edges, side wall, corners of the top edge, portions of the top,  
31 and portions of the bottom of said first floating gate; and

32 a second tunneling zone formed between said second floating  
33 gate and said third control gate, and including one or more of

1 edges, side wall, corners of the top edge, portions of the top,  
2 and portions of the bottom of said second floating gate.

3  
4 2. A memory structure comprising:

5 a source region of a first conductivity type;

6 a drain region of said first conductivity type;

7 a first channel region of a second conductivity type opposite  
8 said first conductivity type, located adjacent said source  
9 region, a portion of said first channel region adjacent said  
10 source region being doped to said second conductivity type to a  
11 dopant concentration greater than that of said first channel  
12 region;

13 a second channel region of said second conductivity type  
14 opposite said first conductivity type, located adjacent said  
15 drain region, a portion of said second channel region adjacent  
16 said drain region being doped to said second conductivity type to  
17 a dopant concentration greater than that of said second channel  
18 region;

19 a transfer channel region of said second conductivity type,  
20 located between said first and second channel regions;

21 a first floating gate located above said first channel  
22 region;

23 a second floating gate located above said second channel  
24 region;

25 a first control gate located above said first floating gate,  
26 serving as a steering element associated with said first floating  
27 gate;

28 a second control gate located above said second floating  
29 gate, serving as a steering element associated with said second  
30 floating gate;

31 a third control gate located above said transfer channel  
32 region, serving as a control gate of an access transistor;

33 a first tunneling zone formed between said first floating  
34 gate and said third control gate, and including one or more of

edges, side wall, corners of the top edge, portions of the top,  
and portions of the bottom of said first floating gate; and  
a second tunneling zone formed between said second floating  
gate and said third control gate, and including one or more of  
edges, side wall, corners of the top edge, portions of the top,  
and portions of the bottom of said second floating gate.

3. A memory structure comprising:  
a source region of a first conductivity type;  
a drain region of said first conductivity type;  
a first channel region of a second conductivity type opposite  
said first conductivity type, located adjacent said source  
region;  
a second channel region of said second conductivity type  
opposite said first conductivity type, located adjacent said  
drain region;  
a transfer channel region of said second conductivity type,  
located between said first and second channel regions;  
a first floating gate located above said first channel  
region;  
a second floating gate located above said second channel  
region;  
a first control gate located above said first floating gate,  
serving as a steering element associated with said first floating  
gate;  
a second control gate located above said second floating  
gate, serving as a steering element associated with said second  
floating gate;  
a third control gate located above said transfer channel  
region, serving as a control gate of an access transistor;  
a first tunneling zone formed between said first floating  
gate and said third control gate, and including one or more of  
edges, side wall, corners of the top edge, portions of the top,  
and portions of the bottom of said first floating gate;

1 a second tunneling zone formed between said second floating  
2 gate and said third control gate, and including one or more of  
3 edges, side wall, corners of the top edge, portions of the top,  
4 and portions of the bottom of said second floating gate;

5 a first doped region at the interface of said first channel  
6 region and said transfer channel region, said first doped region  
7 being doped to said second conductivity type and having a greater  
8 dopant concentration than that of said first channel region and  
9 said transfer channel region; and

10 a second doped region at the interface of said second channel  
11 region and said transfer channel region, said second doped region  
12 being doped to said second conductivity type and having a greater  
13 dopant concentration than that of said second channel region and  
14 said transfer channel region.

15

16 4. A memory array having a plurality of memory cells,  
17 comprising:

18 a plurality of diffused lines running in a first direction,  
19 serving as source and drain regions of said memory cells, each  
20 memory cell having a first channel region located adjacent said  
21 source region and a second channel region located adjacent said  
22 drain region, and a transfer channel region located between its  
23 said first and second channel regions;

24 a plurality of first floating gates, each located above said  
25 first channel region of an associated one of said memory cells;

26 a plurality of second floating gates, each located above said  
27 second channel region of an associated one of said memory cells;

28 a plurality of first control gate lines, running in said  
29 first direction, each located above an associated set of said  
30 first floating gates and serving as steering elements associated  
31 with each said first floating gate;

32 a plurality of second control gate lines, running in said  
33 first direction, each located above an associated set of said

1 second floating gates and serving as steering elements associated  
2 with each said second floating gate; and  
3 a plurality of row lines, running in a second direction  
4 generally perpendicular to said first direction, forming a set of  
5 third control gates above said transfer channel regions of each  
6 memory cell, overlying at least a portion of associated ones of  
7 said first and second control gates and serving as control gates  
8 of access transistors of associated memory cells,  
9 wherein each of said memory cells is associated with the  
10 intersection of one of said diffused lines and one of said row  
11 lines, and  
12 wherein each memory cell includes a first tunnelling zone  
13 formed between said first floating gate and said third control  
14 gate, and including one or more of edges, side wall, corners of  
15 the top edge, portions of the top, and portions of the bottom of  
16 said first floating gate, and  
17 wherein each memory cell includes a second tunnelling zone  
18 formed between said second floating gate and said third control  
19 gate, and including one or more of edges, side wall, corners of  
20 the top edge, portions of the top, and portions of the bottom of  
21 said second floating gate.

22  
23 5. A memory array having a plurality of memory cells,  
24 comprising:

25 a plurality of diffused lines running in a first direction,  
26 serving as source and drain regions of said memory cells, each  
27 memory cell having a first channel region located adjacent said  
28 source region, a portion of said first channel region adjacent  
29 said source region being doped to said second conductivity type  
30 to a dopant concentration greater than that of said first channel  
31 region and a second channel region located adjacent said drain  
32 region, a portion of said second channel region adjacent said  
33 drain region being doped to said second conductivity type to a  
34 dopant concentration greater than that of said second channel

1 region, and a transfer channel region located between its said  
2 first and second channel regions;  
3 a plurality of first floating gates, each located above said  
4 first channel region of an associated one of said memory cells;  
5 a plurality of second floating gates, each located above said  
6 second channel region of an associated one of said memory cells;  
7 a plurality of first control gate lines, running in said  
8 first direction, each located above an associated set of said  
9 first floating gates and serving as steering elements associated  
10 with each said first floating gate;  
11 a plurality of second control gate lines, running in said  
12 first direction, each located above an associated set of said  
13 second floating gates and serving as steering elements associated  
14 with each said second floating gate; and  
15 a plurality of row lines, running in a second direction  
16 generally perpendicular to said first direction, forming a set of  
17 third control gates above said transfer channel regions of each  
18 memory cell, and serving as control gates of access transistors  
19 of associated memory cells,  
20 wherein each of said memory cells is associated with the  
21 intersection of one of said diffused lines and one of said row  
22 lines, and  
23 wherein each memory cell includes a first tunnelling zone  
24 formed between said first floating gate and said third control  
25 gate, and including one or more of edges, side wall, corners of  
26 the top edge, portions of the top, and portions of the bottom of  
27 said first floating gate, and  
28 wherein each memory cell includes a second tunnelling zone  
29 formed between said second floating gate and said third control  
30 gate, and including one or more of edges, side wall, corners of  
31 the top edge, portions of the top, and portions of the bottom of  
32 said second floating gate.  
33

1        6. A memory array having a plurality of memory cells,  
2 comprising:  
3        a plurality of diffused lines running in a first direction,  
4 serving as source and drain regions of said memory cells, each  
5 memory cell having a first channel region located adjacent said  
6 source region and a second channel region located adjacent said  
7 drain region, and a transfer channel region located between its  
8 said first and second channel regions;  
9        a first doped region at the interface of each said first  
10 channel region and said transfer channel region, said first doped  
11 region being doped to said second conductivity type and having a  
12 greater dopant concentration than that of said first channel  
13 region and said transfer channel region;  
14        a second doped region at the interface of each said second  
15 channel region and said transfer channel region, said second  
16 doped region being doped to said second conductivity type and  
17 having a greater dopant concentration than that of said second  
18 channel region and said transfer channel region  
19        a plurality of first floating gates, each located above said  
20 first channel region of an associated one of said memory cells;  
21        a plurality of second floating gates, each located above said  
22 second channel region of an associated one of said memory cells;  
23        a plurality of first control gate lines, running in said  
24 first direction, each located above an associated set of said  
25 first floating gates and serving as steering elements associated  
26 with each said first floating gate;  
27        a plurality of second control gate lines, running in said  
28 first direction, each located above an associated set of said  
29 second floating gates and serving as steering elements associated  
30 with each said second floating gate; and  
31        a plurality of row lines, running in a second direction  
32 generally perpendicular to said first direction, forming a set of  
33 third control gates above said transfer channel regions of each

1 memory cell, and serving as control gates of access transistors  
2 of associated memory cells,

3 wherein each of said memory cells is associated with the  
4 intersection of one of said diffused lines and one of said row  
5 lines, and

6 wherein each memory cell includes a first tunnelling zone  
7 formed between said first floating gate and said third control  
8 gate, and including one or more of edges, side wall, corners of  
9 the top edge, portions of the top, and portions of the bottom of  
10 said first floating gate, and

11 wherein each memory cell includes a second tunnelling zone  
12 formed between said second floating gate and said third control  
13 gate, and including one or more of edges, side wall, corners of  
14 the top edge, portions of the top, and portions of the bottom of  
15 said second floating gate.

16

17 7. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
18 wherein said first conductivity type is N and said second  
19 conductivity type is P.

20

21 8. A memory structure as in claim 7 wherein said second  
22 conductivity type is provided by boron dopants.

23

24 9. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
25 wherein said floating gates comprise a first layer of  
26 polycrystalline silicon, said first control gates comprise a  
27 second layer of polycrystalline silicon, and said third control  
28 gate comprises a third layer of polycrystalline silicon.

29

30 10. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
31 which is capable of storing two or more logical states.

32



1        11. A memory array as in claim 10 wherein said floating  
2 gates establish one of a plurality of predetermined charge levels  
3 for storing a plurality of two or more logical states.  
4

5        12. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
6 wherein said source region and said drain region comprise buried  
7 diffusions.  
8

9        13. A memory structure as in claim 12 which further  
10 comprises a relatively thick dielectric layer overlying said  
11 buried diffusions.  
12

13       14. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
14 wherein said transfer channel is doped to said second  
15 conductivity type to a doped concentration greater than that of  
16 first and second channel regions.  
17

18       15. A memory structure as in claims 1, 2, 3, 4, 5, or 6  
19 wherein said transfer channel is counter doped to said second  
20 conductivity type to a net doped concentration less than that of  
21 first and second channel regions.  
22

23       16. A memory array as in claims 4, 5, or 6 organized into a  
24 plurality of sectors, each sector comprising one or more rows and  
25 organized such that erasure of all cells of a sector is performed  
26 simultaneously.  
27

28       17. A memory array as in claims 4, 5, or 6 organized as a  
29 virtual ground array.  
30

31       18. A memory array as in claims 4, 5, or 6 wherein said one  
32 of first or second floating gates in alternate cells in a given  
33 row are verified simultaneously.  
34

1        19. A memory array as in claim 18 wherein an entire row is  
2 verified utilizing four verification operations.

3

4        20. A memory array as in claims 4, 5, or 6 wherein said one  
5 of first or second floating gates of alternate cells in a given  
6 row are programmed simultaneously by placing data associated with  
7 each memory cell to be programmed on its associated diffused  
8 lines.

9

10       21. A memory array as in claim 20 wherein an entire row is  
11 programmed utilizing four program operations.

12

13       22. A method for forming a memory structure comprising the  
14 steps of:

15       forming a source region of a first conductivity type;

16       forming a drain region of said first conductivity type;

17       forming a first channel region of a second conductivity type  
18 opposite said first conductivity type, adjacent said source  
19 region;

20       forming a second channel region of said second conductivity  
21 type, adjacent said drain region;

22       forming a transfer channel region of said second conductivity  
23 type, between said first and second channel regions;

24       forming a first floating gate above said first channel  
25 region;

26       forming a second floating gate above said second channel  
27 region;

28       forming a first control gate above said first floating gate,  
29 serving as a steering element associated with said first floating  
30 gate;

31       forming a second control gate above said second floating  
32 gate, serving as a steering element associated with said second  
33 floating gate;

1 forming a third control gate above said transfer channel  
2 region, serving as a control gate of an access transistor, said  
3 third control gate also overlying at least a portion of said  
4 first and second control gates;

5 forming a first tunneling zone between said first floating  
6 gate and said third control gate, and including one or more of  
7 edges, side wall, corners of the top edge, portions of the top,  
8 and portions of the bottom of said first floating gate; and

9 forming a second tunneling zone between said second floating  
10 gate and said third control gate, and including one or more of  
11 edges, side wall, corners of the top edge, portions of the top,  
12 and portions of the bottom of said second floating gate.

13

14 23. A method for forming a memory structure comprising the  
15 steps of:

16 forming a source region of a first conductivity type;

17 forming a drain region of said first conductivity type;

18 forming a first channel region of a second conductivity type  
19 opposite said first conductivity type, adjacent said source  
20 region, a portion of said first channel region adjacent said  
21 source region being doped to said second conductivity type to a  
22 dopant concentration greater than that of said first channel  
23 region;

24 forming a second channel region of said second conductivity  
25 type, adjacent said drain region, a portion of said second  
26 channel region adjacent said drain region being doped to said  
27 second conductivity type to a dopant concentration greater than  
28 that of said second channel region;

29 forming a transfer channel region of said second conductivity  
30 type, between said first and second channel regions;

31 forming a first floating gate above said first channel  
32 region;

33 forming a second floating gate above said second channel  
34 region;

1       forming a first control gate above said first floating gate,  
2       serving as a steering element associated with said first floating  
3       gate;  
4       forming a second control gate above said second floating  
5       gate, serving as a steering element associated with said second  
6       floating gate;  
7       forming a third control gate above said transfer channel  
8       region, serving as a control gate of an access transistor;  
9       forming a first tunneling zone between said first floating  
10      gate and said third control gate, and including one or more of  
11      edges, side wall, corners of the top edge, portions of the top,  
12      and portions of the bottom of said first floating gate; and  
13      forming a second tunneling zone between said second floating  
14      gate and said third control gate, and including one or more of  
15      edges, side wall, corners of the top edge, portions of the top,  
16      and portions of the bottom of said second floating gate.  
17  
18      24. A method for forming a memory structure comprising the  
19      steps of:  
20      forming a source region of a first conductivity type;  
21      forming a drain region of said first conductivity type;  
22      forming a first channel region of a second conductivity type  
23      opposite said first conductivity type, adjacent said source  
24      region;  
25      forming a second channel region of said second conductivity  
26      type, adjacent said drain region;  
27      forming a transfer channel region of said second conductivity  
28      type, between said first and second channel regions;  
29      forming a first floating gate above said first channel  
30      region;  
31      forming a second floating gate above said second channel  
32      region;

1       forming a first control gate above said first floating gate,  
2       serving as a steering element associated with said first floating  
3       gate;  
4       forming a second control gate above said second floating  
5       gate, serving as a steering element associated with said second  
6       floating gate;  
7       forming a third control gate above said transfer channel  
8       region, serving as a control gate of an access transistor;  
9       forming a first tunneling zone between said first floating  
10      gate and said third control gate, and including one or more of  
11      edges, side wall, corners of the top edge, portions of the top,  
12      and portions of the bottom of said first floating gate;  
13      a second tunneling zone between said second floating gate and  
14      said third control gate, and including one or more of edges, side  
15      wall, corners of the top edge, portions of the top, and portions  
16      of the bottom of said second floating gate;  
17      forming a first doped region at the interface of said first  
18      channel region and said transfer channel region, said first doped  
19      region being doped to said second conductivity type and having a  
20      greater dopant concentration than that of said first channel  
21      region and said transfer channel region; and  
22      forming a second doped region at the interface of said second  
23      channel region and said transfer channel region, said second  
24      doped region being doped to said second conductivity type and  
25      having a greater dopant concentration than that of said second  
26      channel region and said transfer channel region.  
27  
28      25. A method for forming a memory array having a plurality  
29      of memory cells, comprising the steps of:  
30      forming a plurality of diffused lines running in a first  
31      direction, serving as source and drain regions of said memory  
32      cells, each memory cell having a first channel region located  
33      adjacent said source region and a second channel region located

1 adjacent said drain region, and a transfer channel region located  
2 between its said first and second channel regions;  
3 forming a plurality of first floating gates, each located  
4 above said first channel region of an associated one of said  
5 memory cells;  
6 forming a plurality of second floating gates, each located  
7 above said second channel region of an associated one of said  
8 memory cells;  
9 forming a plurality of first control gate lines, running in  
10 said first direction, each located above an associated set of  
11 said first floating gates and serving as steering elements  
12 associated with each said first floating gate;  
13 forming a plurality of second control gate lines, running in  
14 said first direction, each located above an associated set of  
15 said second floating gates and serving as steering elements  
16 associated with each said second floating gate; and  
17 forming a plurality of row lines, running in a second  
18 direction generally perpendicular to said first direction,  
19 forming a set of third control gates above said transfer channel  
20 regions of each memory cell, overlying at least a portion of  
21 associated ones of said first and second control gates and  
22 serving as control gates of access transistors of associated  
23 memory cells,  
24 wherein each of said memory cells is associated with the  
25 intersection of one of said diffused lines and one of said row  
26 lines, and  
27 wherein each memory cell includes a first tunnelling zone  
28 formed between said first floating gate and said third control  
29 gate, and including one or more of edges, side wall, corners of  
30 the top edge, portions of the top, and portions of the bottom of  
31 said first floating gate, and  
32 wherein each memory cell includes a second tunnelling zone  
33 formed between said second floating gate and said third control  
34 gate, and including one or more of edges, side wall, corners of

1 the top edge, portions of the top, and portions of the bottom of  
2 said second floating gate.

3

4 26. A method of forming a memory array having a plurality of  
5 memory cells, comprising the steps of:

6 forming a plurality of diffused lines running in a first  
7 direction, serving as source and drain regions of said memory  
8 cells, each memory cell having a first channel region located  
9 adjacent said source region, a portion of said first channel  
10 region adjacent said source region being doped to said second  
11 conductivity type to a dopant concentration greater than that of  
12 said first channel region and a second channel region located  
13 adjacent said drain region, a portion of said second channel  
14 region adjacent said drain region being doped to said second  
15 conductivity type to a dopant concentration greater than that of  
16 said second channel region, and a transfer channel region located  
17 between its said first and second channel regions;

18 forming a plurality of first floating gates, each located  
19 above said first channel region of an associated one of said  
20 memory cells;

21 forming a plurality of second floating gates, each located  
22 above said second channel region of an associated one of said  
23 memory cells;

24 forming a plurality of first control gate lines, running in  
25 said first direction, each located above an associated set of  
26 said first floating gates and serving as steering elements  
27 associated with each said first floating gate;

28 forming a plurality of second control gate lines, running in  
29 said first direction, each located above an associated set of  
30 said second floating gates and serving as steering elements  
31 associated with each said second floating gate; and

32 forming a plurality of row lines, running in a second  
33 direction generally perpendicular to said first direction,  
34 forming a set of third control gates above said transfer channel

1 regions of each memory cell, and serving as control gates of  
2 access transistors of associated memory cells,  
3 wherein each of said memory cells is associated with the  
4 intersection of one of said diffused lines and one of said row  
5 lines, and

6 wherein each memory cell includes a first tunnelling zone  
7 formed between said first floating gate and said third control  
8 gate, and including one or more of edges, side wall, corners of  
9 the top edge, portions of the top, and portions of the bottom of  
10 said first floating gate, and

11 wherein each memory cell includes a second tunnelling zone  
12 formed between said second floating gate and said third control  
13 gate, and including one or more of edges, side wall, corners of  
14 the top edge, portions of the top, and portions of the bottom of  
15 said second floating gate.

16  
17 27. A method of forming a memory array having a plurality of  
18 memory cells, comprising the steps of:

19 forming a plurality of diffused lines running in a first  
20 direction, serving as source and drain regions of said memory  
21 cells, each memory cell having a first channel region located  
22 adjacent said source region and a second channel region located  
23 adjacent said drain region, and a transfer channel region located  
24 between its said first and second channel regions;

25 forming a first doped region at the interface of each said  
26 first channel region and said transfer channel region, said first  
27 doped region being doped to said second conductivity type and  
28 having a greater dopant concentration than that of said first  
29 channel region and said transfer channel region;

30 forming a second doped region at the interface of each said  
31 second channel region and said transfer channel region, said  
32 second doped region being doped to said second conductivity type  
33 and having a greater dopant concentration than that of said  
34 second channel region and said transfer channel region;



1       forming a plurality of first floating gates, each located  
2 above said first channel region of an associated one of said  
3 memory cells;  
4       forming a plurality of second floating gates, each located  
5 above said second channel region of an associated one of said  
6 memory cells;  
7       forming a plurality of first control gate lines, running in  
8 said first direction, each located above an associated set of  
9 said first floating gates and serving as steering elements  
10 associated with each said first floating gate;  
11       forming a plurality of second control gate lines, running in  
12 said first direction, each located above an associated set of  
13 said second floating gates and serving as steering elements  
14 associated with each said second floating gate; and  
15       forming a plurality of row lines, running in a second  
16 direction generally perpendicular to said first direction,  
17 forming a set of third control gates above said transfer channel  
18 regions of each memory cell, and serving as control gates of  
19 access transistors of associated memory cells,  
20       wherein each of said memory cells is associated with the  
21 intersection of one of said diffused lines and one of said row  
22 lines, and  
23       wherein each memory cell includes a first tunnelling zone  
24 formed between said first floating gate and said third control  
25 gate, and including one or more of edges, side wall, corners of  
26 the top edge, portions of the top, and portions of the bottom of  
27 said first floating gate, and  
28       wherein each memory cell includes a second tunnelling zone  
29 formed between said second floating gate and said third control  
30 gate, and including one or more of edges, side wall, corners of  
31 the top edge, portions of the top, and portions of the bottom of  
32 said second floating gate.  
33

1        28. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
2 said first conductivity type is N and said second conductivity  
3 type is P.

4

5        29. A method as in claim 28 wherein said second  
6 conductivity type is provided by boron dopants.

7

8        30. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
9 said floating gates comprise a first layer of polycrystalline  
10 silicon, said first control gates comprise a second layer of  
11 polycrystalline silicon, and said third control gate comprises a  
12 third layer of polycrystalline silicon.

13

14        31. A method as in claims 22, 23, 24, 25, 26, or 27 which is  
15 capable of storing two or more logical states.

16

17        32. A method as in claim 31 wherein said floating gates  
18 establish one of a plurality of predetermined charge levels for  
19 storing a plurality of two or more logical states.

20

21        33. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
22 said source region and said drain region comprise buried  
23 diffusions.

24

25        34. A method as in claim 33 which further comprises the step  
26 of forming a relatively thick dielectric layer overlying said  
27 buried diffusions.

28

29        35. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
30 said transfer channel is doped to said second conductivity type  
31 to a doped concentration greater than that of first and second  
32 channel regions.

33

1 36. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
2 said transfer channel is counter doped to said second  
3 conductivity type to a net doped concentration less than that of  
4 first and second channel regions.  
5

6 37. A method as in claims 25, 26, or 27 organized into a  
7 plurality of sectors, each sector comprising one or more rows and  
8 organized such that erasure of all cells of a sector is performed  
9 simultaneously.  
10

11 38. A method as in claims 25, 26, or 27 organized as a  
12 virtual ground array.  
13

14 39. A method as in claims 25, 26, or 27 wherein said one of  
15 first or second floating gates in alternate cells in a given row  
16 are verified simultaneously.  
17

18 40. A method as in claim 39 wherein an entire row is  
19 verified utilizing four verification operations.  
20

21 41. A method as in claims 25, 26, or 27 wherein said one of  
22 first or second floating gates of alternate cells in a given row  
23 are programmed simultaneously by placing data associated with  
24 each memory cell to be programmed on its associated diffused  
25 line.  
26

27 42. A method as in claim 20 wherein an entire row is  
28 programmed utilizing four program operations.  
29

30 43. A method as in claims 22, 23 or 24 wherein said steps of  
31 forming said first floating gate and said first control gate, and  
32 said second floating gate and said second control gate comprising  
33 the steps of:

1 forming a plurality of polycrystalline silicon strips in a  
2 first direction above and insulated from said first and second  
3 channel regions;

4 forming a layer of polycrystalline silicon above and  
5 insulated from said plurality of polycrystalline silicon strips;  
6 and

7 patterning said plurality of polycrystalline silicon strips  
8 and said layer of polycrystalline silicon into strips running in  
9 a second direction generally perpendicular to said first  
10 direction in order to form said first and second floating gates  
11 and said first and second control gates.

12

13 44. A method as in claims 25, 26, or 27 wherein said steps  
14 of forming said first floating gate and said first control gate,  
15 and said second floating gate and said second control gate  
16 comprising the steps of:

17 forming a plurality of polycrystalline silicon strips in said  
18 second direction above and insulated from said first and second  
19 channel regions;

20 forming a layer of polycrystalline silicon above and  
21 insulated from said plurality of polycrystalline silicon strips;  
22 and

23 patterning said plurality of polycrystalline silicon strips  
24 and said layer of polycrystalline silicon into strips running in  
25 said first direction in order to form said first and second  
26 floating gates and said first and second control gates.

27

28 45. A method as in claim 43 wherein said step of patterning  
29 said plurality of polycrystalline silicon strips and said layer  
30 of polycrystalline silicon is performed using the minimum feature  
31 lithographic width available in the fabrication process.

32

33

34

1        46. A method as in claim 44 wherein said step of patterning  
2 said plurality of polycrystalline silicon strips and said layer  
3 of polycrystalline silicon is performed using the minimum feature  
4 lithographic width available in the fabrication process.

5

6        47. A method as in claims 22, 23, 24, 25, 26, or 27 wherein  
7 said step of forming said transfer channel region and said source  
8 and drain regions comprises the step of delineating said transfer  
9 channel region and said source and drain regions simultaneously.

10

11        48. A method as in claim 47 wherein said step of  
12 simultaneously delineating said transfer channel region and said  
13 source and drain regions is performed utilizing the minimum  
14 lithographic space between features available in the fabrication  
15 process.

16

17        49. A method as in claims 22, 23, 24, 25, 26, or 27 which  
18 further comprises the step of forming a tunnel oxide on only the  
19 edges of said first floating gate and said second floating gate  
20 adjacent to said transfer channel region.

21

22        50. A method as in claims 25, 26, or 27 which further  
23 comprises the step of forming a tunnel oxide on only the edges of  
24 said first floating gate and said second floating gate adjacent  
25 to said transfer channel region to serve as said tunneling zones,  
26 comprising the steps of:

27        forming a plurality of polycrystalline silicon strips;

28        forming a second layer of polycrystalline silicon above and  
29 insulated from said first layer of polycrystalline silicon;

30        patterning said second layer of polycrystalline silicon to  
31 form said plurality of said first and second control gates;

32        patterning said first layer of polycrystalline silicon to  
33 remove portions of said first layer of polycrystalline silicon  
34 between adjacent pairs of said first and second control gates;

forming spacer dielectric on the exposed side walls of said first and second polycrystalline silicon layers;  
removing exposed portions of said first polycrystalline silicon layer;  
forming tunnel oxide on the exposed side walls of said first polycrystalline silicon layer; and  
forming a third layer of polycrystalline silicon.

51. A method as in claim 50 wherein a portion of said first and second channel regions adjacent said source regions and drain regions, respectively, are doped to concentrations greater than that of the remaining portions of said channel regions prior to said step of forming spacer dielectric and said source and drain regions are formed after said step of forming said spacer dielectric.

52. A memory array comprising a plurality of segments, each segment including a subarray comprising:

a plurality of adjacent bit lines running in a first direction to form a corresponding plurality of columns;

a plurality of steering lines running in said first direction;

a plurality of word lines running in a second direction generally perpendicular to said first direction to form a corresponding plurality of rows; and

a plurality of memory cells, each memory cell being associated with the intersection of one of said bit lines and one of said word lines.

53. A structure as in claim 52 wherein said word lines serve as said erase lines.

54. A structure as in claim 53 which includes one or more sectors, each sector containing one or more of said word lines

1 and their corresponding erase lines, each said sector containing  
2 a plurality of memory cells capable of being simultaneously  
3 erased.

4  
5 55. A structure as in claim 53 which includes one or more  
6 sectors, each sector containing one or more of said word lines  
7 which also serve as erase lines, each said sector containing a  
8 plurality of memory cells capable of being simultaneously erased.

9  
10 56. A method as in claim 52 which further comprises the step  
11 of storing one of two or more logical states in said memory cell.

12  
13 57. A memory array as in claim 52 organized as a virtual  
14 ground array.

15  
16 58. A memory array as in claim 52 which further comprises:  
17 a plurality of diffused lines running in said first  
18 direction, serving as said bit lines and forming source and drain  
19 regions of said memory cells, each memory cell having a first  
20 channel region located adjacent said source region and a second  
21 channel region located adjacent said drain region, and a transfer  
22 channel region located between its said first and second channel  
23 regions;

24 a plurality of first floating gates, each located above said  
25 first channel region of an associated one of said memory cells;

26 a plurality of second floating gates, each located above said  
27 second channel region of an associated one of said memory cells;

28 a plurality of first control gate lines, running in said  
29 first direction, each located above an associated set of said  
30 first floating gates and serving as those of said steering lines  
31 associated with each said first floating gate;

32 a plurality of second control gate lines, running in said  
33 first direction, each located above an associated set of said

1 second floating gates and serving as those of said steering lines  
2 associated with each said second floating gate; and  
3 a plurality of row lines serving as said word lines, running  
4 in said second direction generally perpendicular to said first  
5 direction, forming a set of third control gates above said  
6 transfer channel regions of each memory cell, overlying at least  
7 a portion of associated ones of said first and second control  
8 gates and serving as control gates of access transistors of  
9 associated memory cells,

10 wherein each of said memory cells is associated with the  
11 intersection of one of said diffused lines and one of said row  
12 lines, and

13 wherein each memory cell includes a first tunnelling zone  
14 formed between said first floating gate and said third control  
15 gate, and including one or more of edges, side wall, corners of  
16 the top edge, portions of the top, and portions of the bottom of  
17 said first floating gate, and

18 wherein each memory cell includes a second tunnelling zone  
19 formed between said second floating gate and said third control  
20 gate, and including one or more of edges, side wall, corners of  
21 the top edge, portions of the top, and portions of the bottom of  
22 said second floating gate.

23  
24 59. A memory array as in claim 58 wherein said one of first  
25 or second floating gates in alternate cells in a given row are  
26 verified simultaneously.

27  
28 60. A memory array as in claim 59 wherein an entire row is  
29 verified utilizing four verification operations.

30  
31 61. A memory array as in claim 58 wherein alternate cells in  
32 a given row are programmed simultaneously by placing data  
33 associated with each memory cell to be programmed on its  
34 associated bit line.



1        62. A memory array as in claim 61 wherein an entire row is  
2 programmed utilizing four program operations.

3

4        63. A structure as in claims 1, 2, 3, 4, 5, 6, or 52 which  
5 further comprises steering bias circuitry capable of providing  
6 steering bias voltage levels less than zero.

7